SEATTLE COMPUTER
1114 Industry Dr. Seattle WA 98188 206/575-1830

8086 CPU Board

Model 210

For the S-100 Bus

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For the S-100 Bus

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Part Number 900-000799

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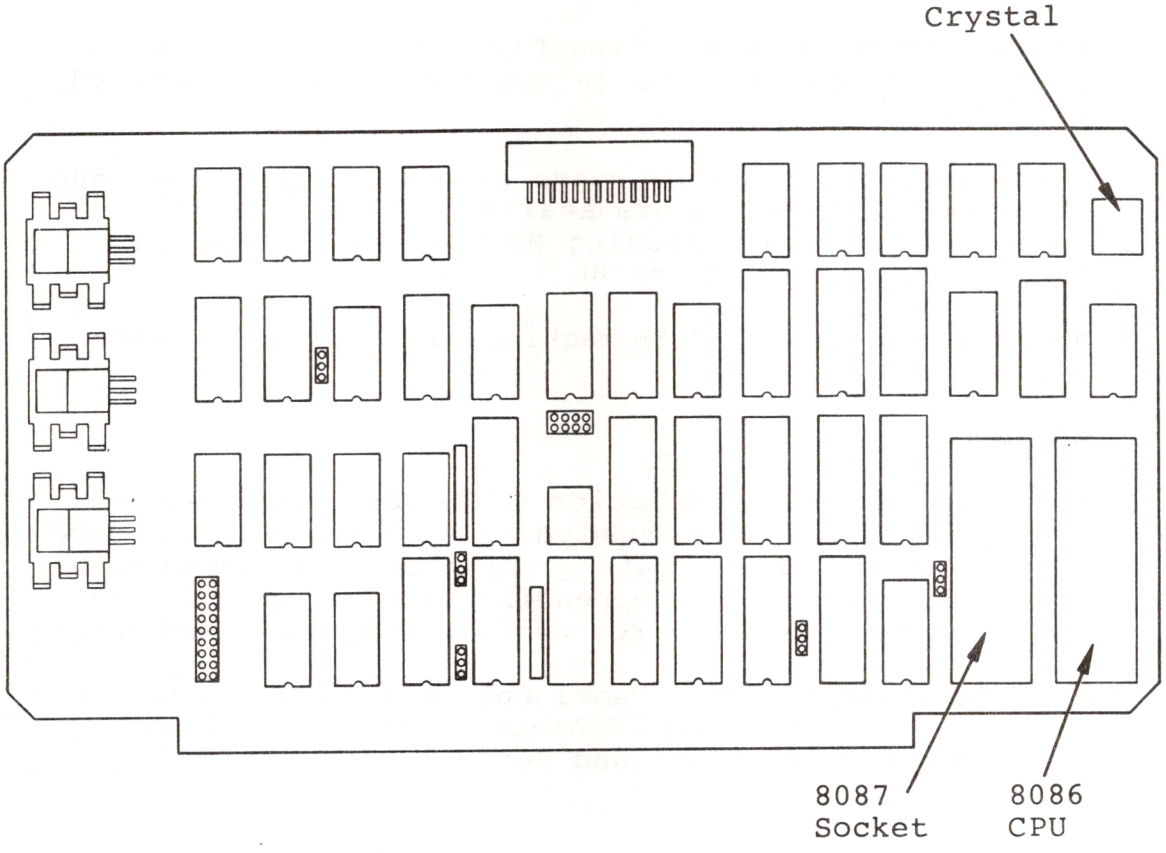
CHAPTER 1. INTRODUCTION

The advanced design of the Seattle Computer Products' 8086 CPU board delivers true 16-bit performance to the S-100 bus. This CPU board can be used as a stand-alone CPU or it can be used together with the SCP-301 CPU Support board.

CPU BOARD MODELS

Two versions of the board are available:

- 10 MHz CPU board (part number 0021001)
- 8 MHz CPU board (part number 0021002)



CPU BOARD FEATURES

- **CPU Chip** - 8086-1 specified at 10 MHz. 8 MHz version also available for use with 8 MHz 8087 numeric data processor. (The 10 MHz version has a 30 MHz crystal; the 8MHz version has a 24 MHz crystal.) For additional details on the CPU chip, see The 8086 Family User's Manual from Intel.

- **IEEE S-696 Standard (S-100)** - Fully compatible with IEEE-696 specifications.

- **Memory Compatibility** - Can use 150 ns dynamic RAMs without wait states. However, static memory is recommended unless the dynamic memory is designed specifically for this CPU.

- **8-Bit/16-Bit Capability** - Can operate with either 8-bit or 16-bit peripherals. This means that older 8-bit memory, disk controllers, and video units can be used with somewhat lower performance.

- **Large address space** - Directly addresses up to one megabyte of memory up to 16 Megabytes through on-card programmable latch.

- **Software Support** - Wide range of operating systems and programming languages are available from Seattle Computer Products including MS-DOS, BASIC, FORTRAN, Pascal, COBOL, and Macro 86.

- **Machine Language** - 8086 machine language instruction set.

- **Options** -

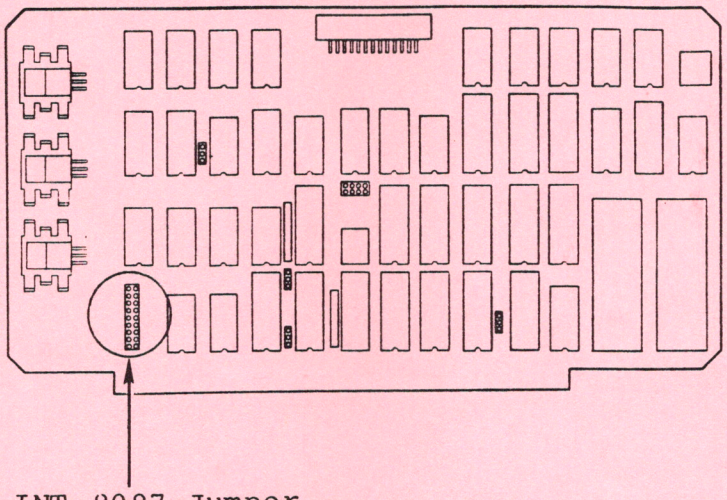
  - **High Speed Math Option** - The 8087 numerical co-processor can be mounted in a socket on the board allowing full floating point and high speed math performance. See Appendix C for information on ordering an 8087 from Seattle Computer Products.

  - **Imsai-Style Front Panel Option** - Socket provided that allows using IMSAI-style front panel for system development and debugging.

CORRECTION

SEATTLE COMPUTER PRODUCTS 8086 CPU BOARD MODEL 210

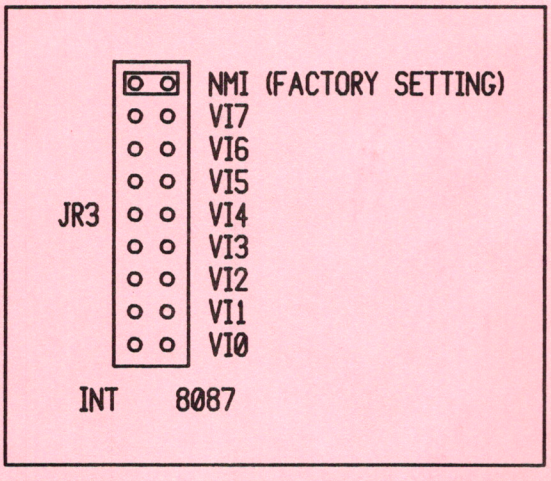
The INT 8087 jumper (jumper JR3) is labelled incorrectly on your 8086 CPU board. This jumper is located near the lower left corner of the CPU board, as shown below:



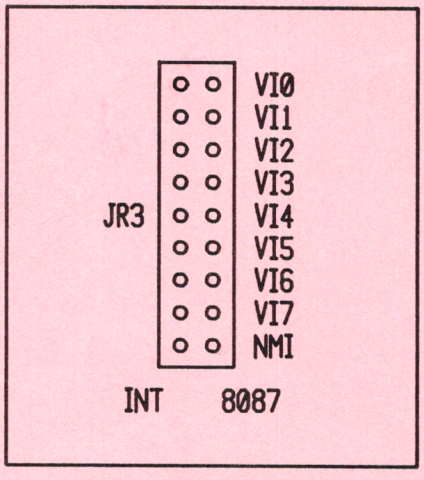
INT 8087 Jumper

The jumper settings should be labelled as shown below. When you receive your board from Seattle Computer, the shunt should be placed over the top two jumper pins (which is incorrectly labelled **VIO** on your board but should be labeled **NMI**). (See page 4 of the 8086 CPU Board Model 210 manual for a description of these jumper settings.)

CORRECT



INCORRECT



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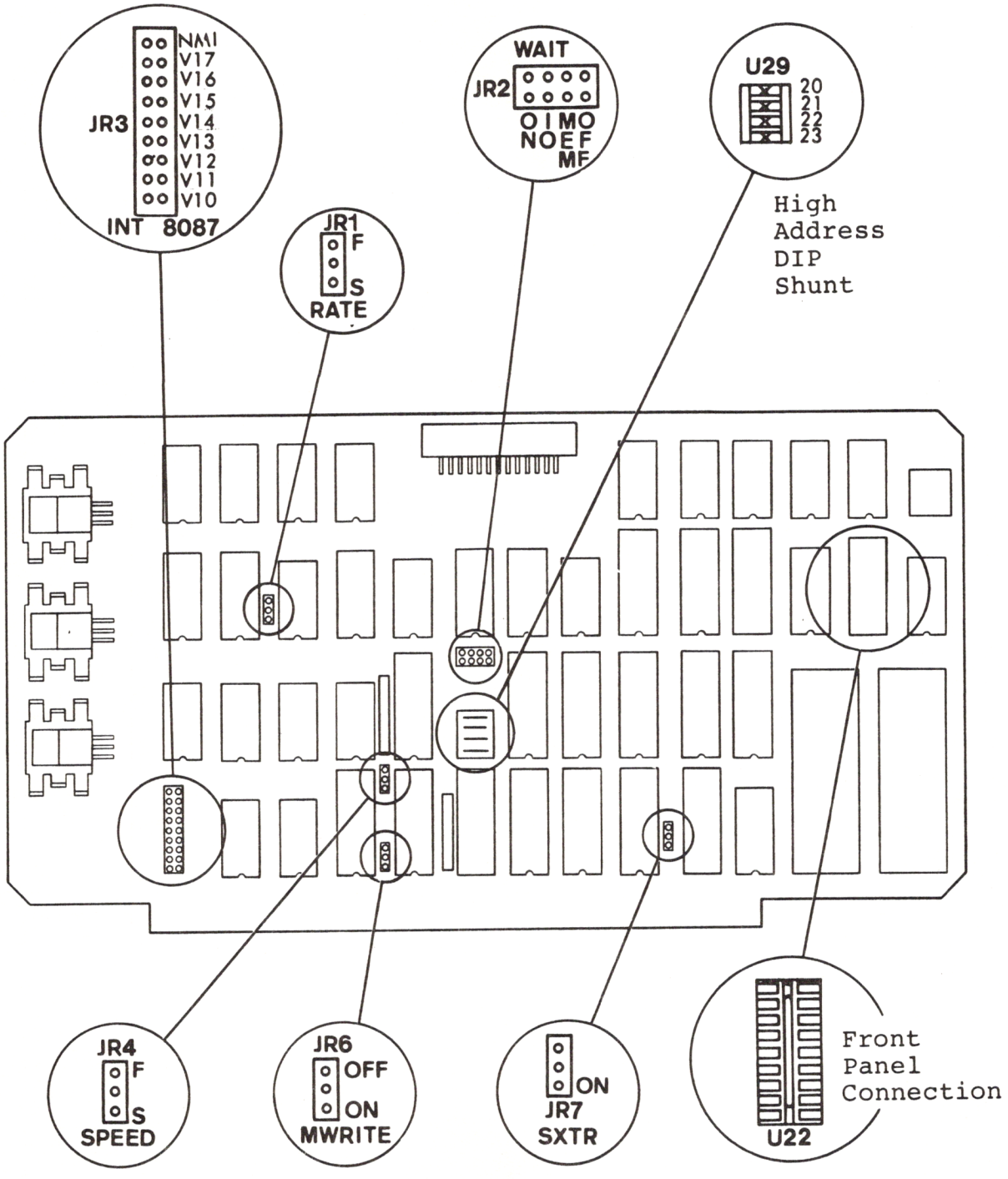
CHAPTER 2. JUMPER SETTINGS



Jumper Settings

RATE JUMPER (JR1)

The RATE jumper position is selected based on the frequency of the crystal on the board.

F — 30 MHz crystal. Used for 10 MHz systems. This is the factory setting for the 10 MHz CPU board (model 0021001).

S — 24 MHz crystal. Used for 8 MHz systems. This is the factory setting for the 8 MHz CPU board (model 0021002).

WAIT JUMPER (JR2)

The WAIT jumper can automatically insert one wait state, allowing more time for the memory or I/O device to respond.

ON — Insert one wait state for both memory and I/O operations.

IO — Insert one wait state for every I/O access.

MEM — Insert one wait state for every memory access.

OFF — Do not insert wait states. This is the factory setting.

INT 8087 JUMPER (JR3)

If an 8087 chip is installed on your board, this jumper selects which S-100 vectored interrupt line or non-masking interrupt is driven when the 8087 requests an interrupt.

If you choose one of the vectored interrupt lines (VI0-VI7), make sure that they are not used by the operating system. (See the MS-DOS Programmer's Reference Manual for details.)

VI0-VI7 — Select vectored interrupt line VI0 through VI7 if an 8087 is installed.

NMI — Select non-masking interrupt if an 8087 is installed. This is the factory setting and is also the correct setting if no 8087 is installed.

SPEED JUMPER (JR4)

The SPEED jumper selects whether the board is running fast (at full speed) or slow (at half speed).

F	Running at full speed (10 MHz for a model 0021001 board or 8 MHz for a model 0021002 board). This is the factory setting.
S	Running at half speed (5 MHz for a model 0021001 board or 4 MHz for a model 0021002 board).

MWRITE JUMPER (JR6)

The MWRITE jumper lets you disconnect the MWRITE (memory write) signal from the S-100 bus if MWRITE is to generated elsewhere in the system.

OFF	CPU board does not generate the MWRITE S-100 signal for all devices.
ON	CPU board generates MWRITE. MWRITE must be generated somewhere else in the system. This is the factory setting.

SXTRQ JUMPER (JR7)

This jumper connects or disconnects the SXTRQ signal (16-bit transfer request) so that the board can operate in 16-bit mode or 8-bit mode.

OFF	8-bit mode
ON	16-bit mode. This is the factory setting.

HIGH ADDRESS DIP SHUNT (U29)

This DIP shunt, which is installed at the factory, connects address bits 20 through 23. It may be removed to disconnect address bits 20 through 23 if they are driven elsewhere in the system.

(Address bits 20 through 23 are used only if more than one megabyte of memory is installed or mapped.)

FRONT PANEL CONNECTOR SOCKET (U22)

This socket allows connection of an IMSAI-type front panel to run, stop, single step, and observe address and data. This socket contains the signals INDISABLE* and OUTDISABLE* which disable the CPU regular bus controls to let you set starting addresses and data.

CHAPTER 3. S-100 CONNECTOR LAYOUT

Pin	Name	Pin	Name	Pin	Name
1	+8 Volts	35	DO1	68	MWRITE
2	+16 Volts	36	DO0	69	
3	XRDY	37	A10	70	0 Volts
4	VI0*	38	DO4	71	
5	VI1*	39	DO5	72	RDY
6	VI2*	40	DO6	73	INT*
7	VI3*	41	DI2	74	HOLD*
8	VI4*	42	DI3	75	RESET*
9	VI5*	43	DI7	76	pSYNC
10	VI6*	44	sM1	77	pWR*
11	VI7*	45	sOUT	78	pDBIN
12	NMI*	46	sINP	79	A0
13		47	sMEMR	80	A1
14		48	sHLTA	81	A2
15	A18	49	CLOCK	82	A6
16	A16	50	GROUND	83	A7
17	A17	51	+8 Volts	84	A8
18	SDSB*	52	-15 Volts	85	A13
19	CDSB*	53	0 Volts	86	A14
20	O Volts	54	SLAVE CLR*	87	A11
21		55		88	DO2
22	ADSB*	56		89	DO3
23	DODSB*	57		90	DO7
24	Φ	58	sXTRQ*	91	DI4
25	pSTVAL*	59	A19	92	DI5
26	pHLDA	60	SIXTN*	93	DI6
27		61	A20	94	DI1
28		62	A21	95	DI0
29	A5	63	A22	96	sINTA
30	A4	64	A23	97	sWO*
31	A3	65		98	SPEED
32	A15	66		99	POC*
33	A12	67		100	GROUND
34	A9				

CHAPTER 4. AC CHARACTERISTICS

In the table on the next page, the symbol in the left column has this form:

Taybz

where: **T** means a timing measurement

a and **b** are abbreviations of signal names

y and **z** are abbreviations of signal levels

The following abbreviations are used:

Signal Names (a,b)	Signal Levels (y,z)
A - Address bus C - CLOCK (Φ) D - pDBIN I - DATA-in M - MWRITE O - DATA-out R - Ready (RDY/XRDY/SIXTN*) S - Status bus V - pSTVAL* W - pWR* Y - pSYNC	H - High L - Low V - Valid X - Invalid

Taybz represents the time interval between

The time when the first signal (a) reaches the y level and

The time when the second signal (b) reaches the z level.

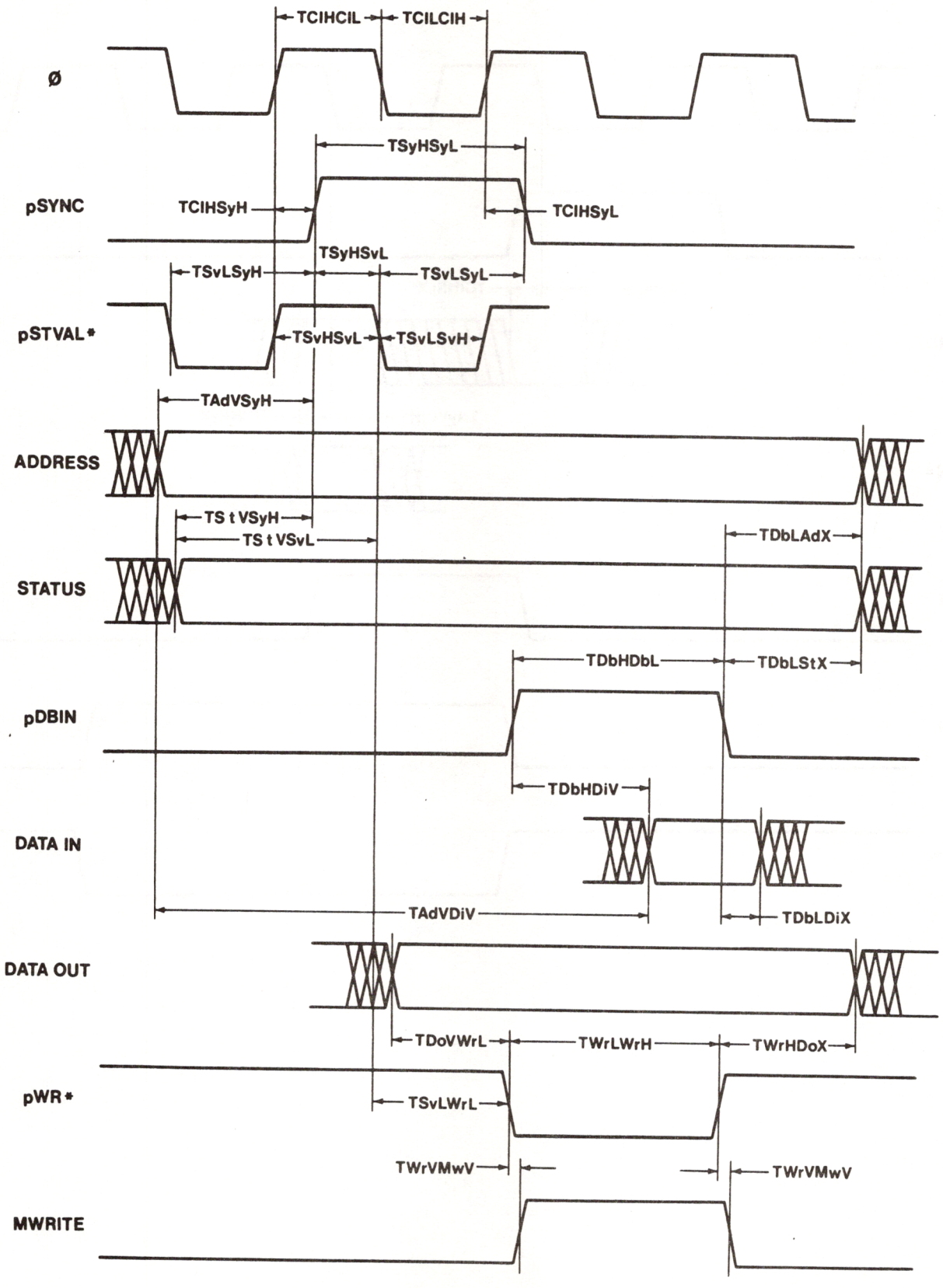
For example, TRVCH means "Time between READY becoming Valid and CLOCK going High."

Times specified are in nanoseconds, either minimum or maximum as appropriate for a worst-case specification. Times listed are for a 5 MHz, an 8 MHz, and a 10 MHz clock, and for comparison, the requirements of the S-100 standard at 4 MHz. The maximum clock speed covered by the standard is 6 MHz.

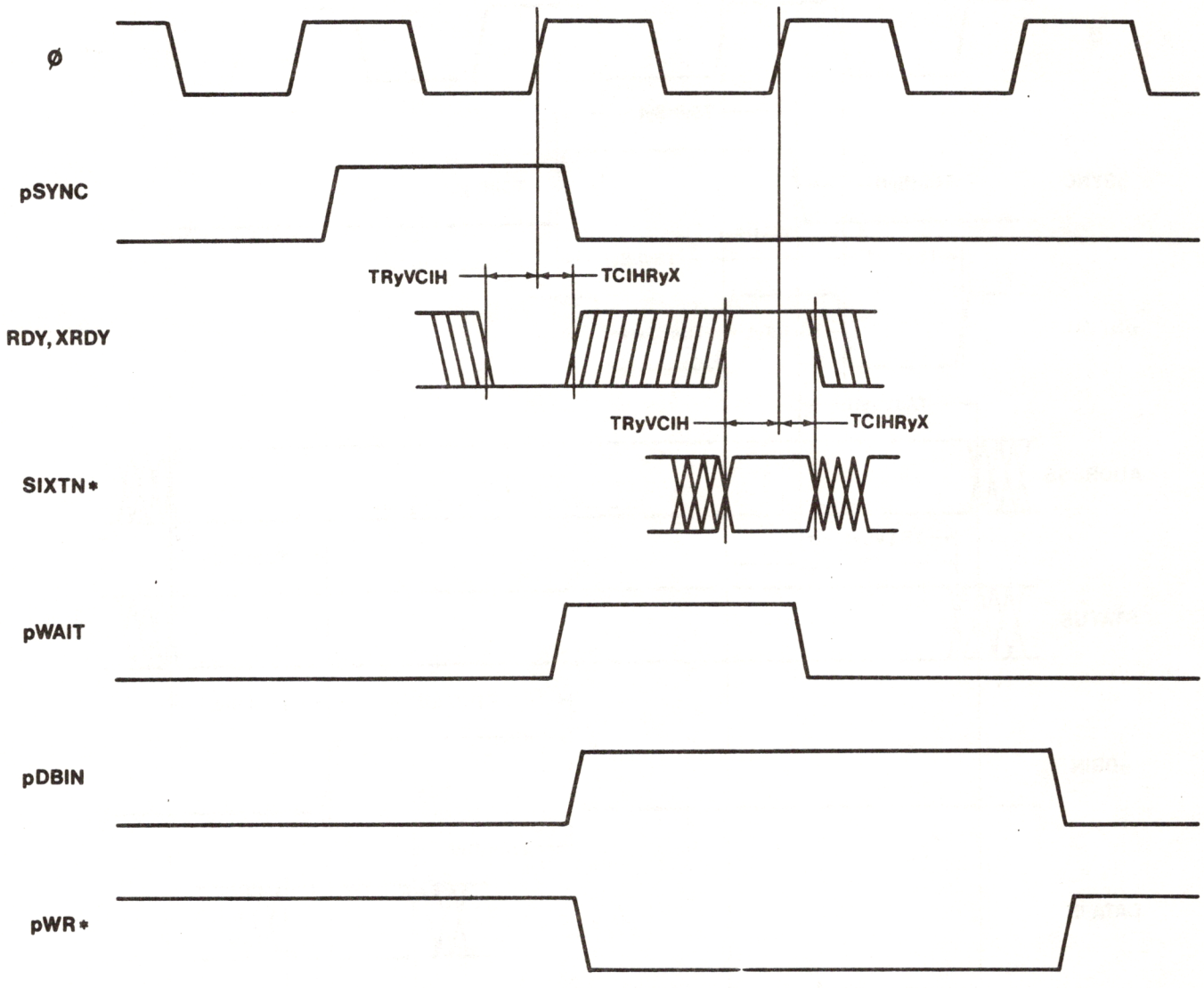
Timing Requirements

Symbol	Description	5 MHz	10 MHz	4 MHz	8 MHz
Inputs					
TAVIV	Allowed address access time	445	220	-	260
TVLIV	Access time from pSTVAL*	280	140	-	130
TRVCH	RDY/XRDY/SIXTN* setup time	70	70	80	50
TCHRX	RDY/XRDY/SIXTN* hold time	0	0	70	0
TDLIX	Data-in hold time	0	0	50	0
TDHIV	Driver enable time for slaves	280	140	50	50
Outputs					
TCLCL, TCHCH	Clock period	200	100	250	125
TCHCL, TCLCH	Clock pulse width	100	50	113	58
TCHYH, TCHYL	Clock to pSYNC delay	20	20	100	20
TYHYL	pSYNC pulse width	90	40	175	115
TVLYL	pSTVAL* low before pSYNC low	56	23	0	62
TVHVL	pSTVAL* pulse width high	106	53	50	58
TVLVH	pSTVAL* pulse width low	80	39	50	58
TVLYH	pSTVAL* low before pSYNC high	56	23	0	62
TYHVL	pSYNC high before pSTVAL* low	144	77	50	45
TAVYH	Address valid before pSYNC	100	50	-	60
TSVYH	Status valid before pSYNC	36	4	-	35
except sXTRQ*		44	8	-	0
TSVVL	Status valid before pSTVAL* low	188	81	40	50
TDLAX, TDLSX	Address/status hold after pDBIN	100	50	50	80
TDHDL	pDBIN pulse width	290	145	225	115
TWLWH	pWR* pulse width	195	95	225	115
TVLWL	pSTVAL* low before pWR* low	67	33	30	62
TOVWL	Data-out setup time before pWR*	156	56	25	45
TWHOX, TWHAX, TWHSX	Data-out/address/status hold	100	50	50	80
TWLMH, TWHML	MWRITE delay from pWR*	30	30	30	30

STANDARD BUS CYCLE



BUS CYCLE WITH ONE WAIT STATE



CHAPTER 5. THEORY OF OPERATION

The signals and functions described below are shown in the schematic in Appendix A. Key signals and timing are shown in the timing diagrams in Appendix B. General and subtle operations are discussed; straightforward functions are left to the reader.

CLOCK CIRCUITRY

The CPU clock is generated by a crystal-controlled logic oscillator constructed of LS 04 inverters with the crystal and resistors and capacitors to insure primary crystal mode operation. Depending on the position of the jumper J4, the oscillator signal directly (fast), or divided by one D flip-flop (slow), appears at U2, pin 13, for full or half speed selection. U2-13 then provides the clock source for the rest of the system. U11 is connected by jumper J1 to provide the 2 mhz S-100 clock signal. See the System Clock Diagram in Appendix B for U11 operation.

U2-13 drives two JK phases and a D flip-flop in a ring counter to produce phased internal clocks for the CPU and general timing. Since the JK and D flip-flops trigger on the opposite clock edge, PHI1 and the CPU CLK are one-half of the clock out of phase allowing time separate triggers for other functions.

CPU CYCLE

The 8086 is operated in a "max" mode (see the Intel product description). The start of a bus cycle is therefore indicated by at least one of the CPU status lines, S0, S1, or S2 assuming a low state. The first activity on all bus cycles is the output and latch function of the address lines. The ALE signal is used to latch the CPU-generated address on the low-going ALE transition. ALE is driven high initially by power on reset in preparation for the first cycle, and thereafter by the CLEAR signal ending each bus cycle. Since ALE is used as the latch signal for the address latches (U30, U40, and U42), this early timing for ALE setting gives maximum setup time.

The first read cycle, shown in the Basic Timing diagram in Appendix B, illustrates this timing. As shown in the diagram, the CPU status bits are OR'd to yield a signal called START, which in turn resets ALE (strobing the address latches) and creates CYCLE which starts U13 as a shift register counter and U1 as the status time counter. U13 creates a 4-step shift output, T1 through T4, which marks the CPU cycle and creates the CLEAR signal to end it. The S-100 SYNC signal marking the beginning of a bus cycle is generated from T1.

During T2, either pDBIN for a bus read or PWR* for a bus write is generated to control the bus data. The logic creating pDBIN stretches the leading edge half a clock cycle to allow maximum data settling time and also time for an addressed peripheral to respond with not ready if it does not have the data available without a wait state.

During T2 the reset is removed from U4 13, the D flip-flop driven by RDY. If a wait state is required (a RDY signal is low), then U4-9 is set high in time to stop the CPU cycle in T3, thus beginning wait states (Tw) until U4-9 again resets. This insures internal control of ready timing, thus only requiring external generation of RDY low in time to catch the CPU clock edge in T2. When U4-9 is set, its Q* side, U4-8, drives the T clock shift register to freeze the T2 state until ready is released. U6-4 drops the ready signal to the CPU, thus causing it to enter wait.

In all cases, U1 creates a strobe (pSTVAL) synchronized with SYNC which indicates that the bus address and status signals are valid.

8-BIT TRANSFERS

During normal 16-bit bus transfers, the signal sXTRQ* is asserted and all peripherals capable of 16-bit transfers respond by holding SXTN* low. In this case the DONE flip-flop stays set and a single bus cycle occurs, as described above.

When an 8-bit transfer is to be made (odd address or 8-bit only peripheral), SXTN* stays high. When SYNC is then high, the logic driving DONE causes DONE to reset and U15-5 resets with it. DONE resets during T2 and drives U6-4 to place the CPU in a wait state. DONE also inhibits the CLEAR signal, allowing the T1-T4 shift counter to run a second cycle. During the first cycle the ODDBT flip-flop sets which then inhibits the SYNC input from reseting DONE. The second recurrence of SYNC then directly sets U15-5, allowing DONE to set during the second cycle for a normal end.

ODDBT (and the other control signals) drive the U19 programmed logic array (PAL) to create the required gating signals to control the S-100-to-8086 bus gating for input or output, depending on the cycle in progress (U18, U32, U33, and U34). These signals are as follows:

Type of Cycle	Signal	Function Enabled
8-bit even read	GC* GA*	DI data to AD0-AD7 input Incidental, DI to AD8-AD15.
8-bit odd read	GA* GE*	DI data to AD8-AD15 input Incidental, U18 to AD0-AD7.
16-bit read, even address	GA* GB*	DI data to AD8-AD15 odd input DO data to AD0-AD7 even input
First byte, odd address read	GC* GA*	DI data to U18, odd input Incidental, DI to AD8-AD15.
Second byte, odd address read	GA* GE*	DI data to AD8-AD15, even input U18 data to AD0-AD7, odd input
8-bit even write	GB* GA*	AD0-AD7 data to DO, output Incidental, AD8-AD15 to DI.
8-bit odd write	GD* GA*	AD8-AD15 data to DO, output Incidental, AD8-AD15 to DI.
16-bit write, even address	GA* GB*	AD8-AD15 data to DI, odd output AD0-AD7 data to DO, even output
First byte, odd address write	GB* GA*	AD0-AD7 data to DO, even output Incidental, AD8-AD15 to DI.
Second byte, odd address write	GD* GA*	AD8-AD15 data to DO, odd output Incidental, AD8-AD15 to DI.

HOLD CYCLES

The 8086 CPU hold sequence requires an external device to initiate hold by inserting a pulse on the RQ/GT0 signal line. When the 8086 is ready for the cycle, it responds by pulsing the same signal line again. When the external hold cycle is complete, the external device pulses RQ/GT0 a third time to signal the 8086 it may have the bus back.

This sequence is controlled by the U25 D flip-flop pair. The S-100 HOLD* signal drives the D input of the first flip-flop, which in turn drives the second flip-flop. Both flip-flops normally remain in the set state. When a hold cycle is requested, HOLD* is held low by the external source. On the next bus clock, the first U25 flip-flop resets, and its Q* and the Q of the second flip-flop drive U24 to produce a low at U24, pin 6, for one clock period. U24 pin 6 is collector OR'd with the CPU and U24 pin 8, pulled up by a resistor, and all drive RQ/GT0. On the next bus clock after the first U25 flip-flop resets, the second U25 flip-flop resets, and the RQ/GT0 pulse is removed. At the same time the reset is removed from U14-10.

When the CPU responds with its own pulse on RQ/GT0, U14-5 sets high driving the pHLDA signal on the S-100 bus which indicates that the requesting device may use the bus. The CPU floats its bus signals before pulsing RQ/GT0. When the external device is done with the bus, it raises HOLD* and the U25 flip-flop sequence is set again, in the process producing one more pulse at U24-8, thus signalling the CPU cycle done.

INTERRUPT CYCLE

Interrupts are initiated as a signal on either the CPU NMI (non maskable interrupt) or the INTR (interrupt) input. In either case an interrupt cycle is initiated following the specifications described in the Intel 8086 Data Sheet. This requires a bus cycle (or two depending on type) from the requesting device and follows all of the rules laid out in the 8086 Data Sheets.

S-100 STATUS

The CPU status signals, S0*, S1*, S2*, and BHE* (bus high enable) are used to generate status for the S-100 bus. The CPU signals are latched in U20 along with the low order address bit (which indicates even or odd address operations for 16-bit transfers) AD0, and the hex address FF which is used as a device select for controlling the high order four address bits, A20 through A23, when so desired under program control (see U21). U44 is a dual 2- to 4- line decoder used to decode the CPU status bits to generate the S-100 status lines. This decoding is as follows:

S2*	S1*	S0*	Cycle Type	sMEMR	sINP	sM1	sOUT	sHLTA	sWO*	sINTA
0	0	0	Interrupt Ack.	0	0	1	0	0	1	1
0	0	1	I/O Read	0	1	0	0	0	1	0
0	1	0	I/O Write	0	0	0	1	0	0	0
0	1	1	CPU Halt	0	0	0	0	1	1	0
1	0	0	Instruc-tion Read	1	0	1	0	0	1	0
1	0	1	Memory Read	1	0	0	0	0	1	0
1	1	0	Memory Write	0	0	0	0	0	0	0
1	1	1	No Operation	-	-	-	-	-	-	-

The eighth S-100 signal, sXTRQ*, which requests 16-bit transfers, is generated by U7 OR'ing together the latched low address bit, BHE*, and interrupt acknowledge. When these are all low, a 16-bit transfer is assumed to an even address. BHE* being high indicates a transfer to an odd address, as does AD0. All interrupt acknowledge cycles ask for a byte response vector, and are therefore 8-bit transfers.

The S-100 status signals are driven to the S-100 bus with drivers, U43, part of U26, U38, and U37, which allows these signals to be tristated under bus control by the signals sDSB* (disable status bus), DODSB* (disable output bus), CDSB* (disable control signals), and ADSB* (disable address bus).

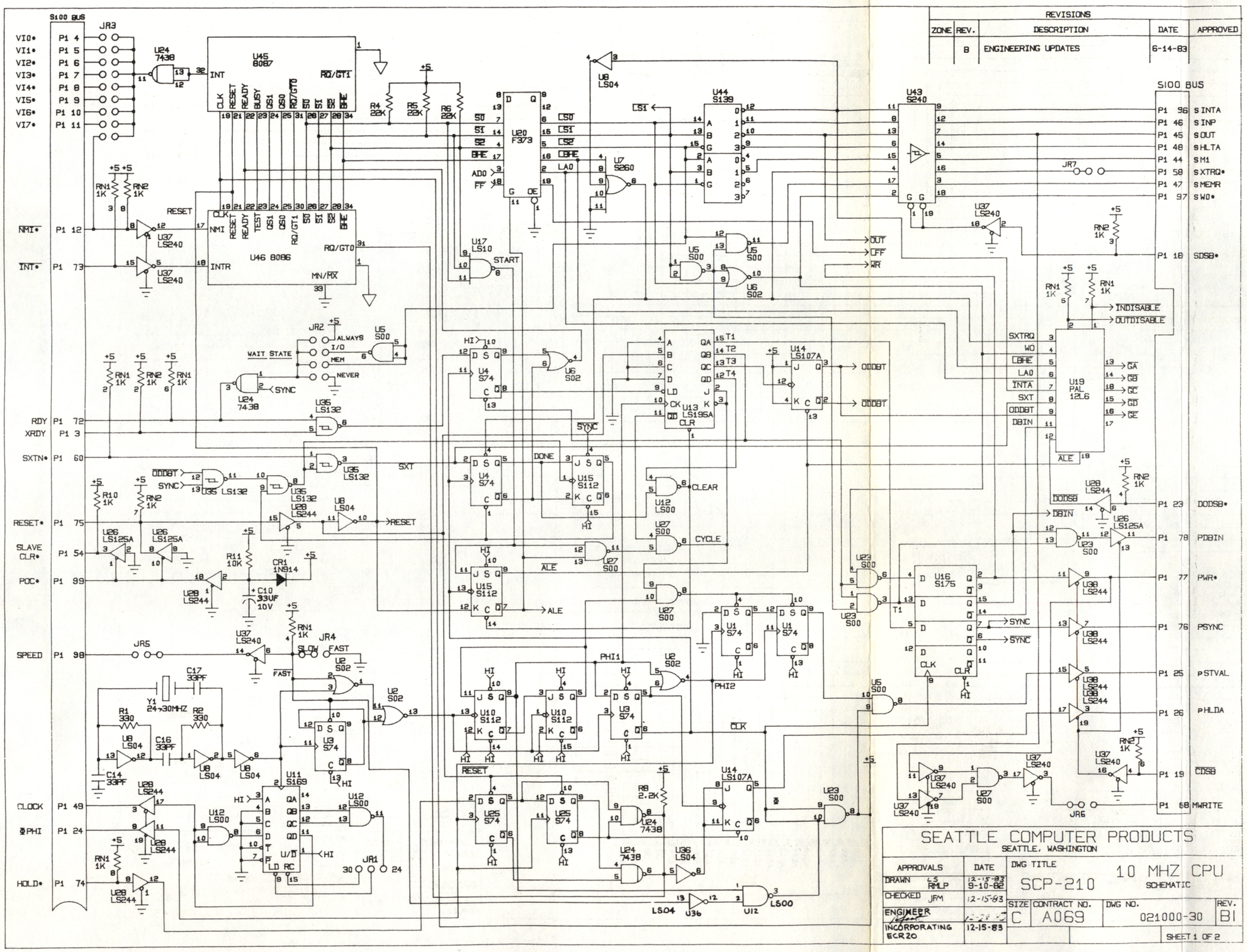
RESET

Power on clear (POC*) and reset functions (RESET*) are implemented from the S-100 bus. POC* is generated by the CPU card on power up and drives both RESET* and SLAVE CLR* to provide system wide reset. An external source may drive RESET* to cause the CPU to restart. This signal should be at least 10 milliseconds in duration to insure everything is initiated properly.

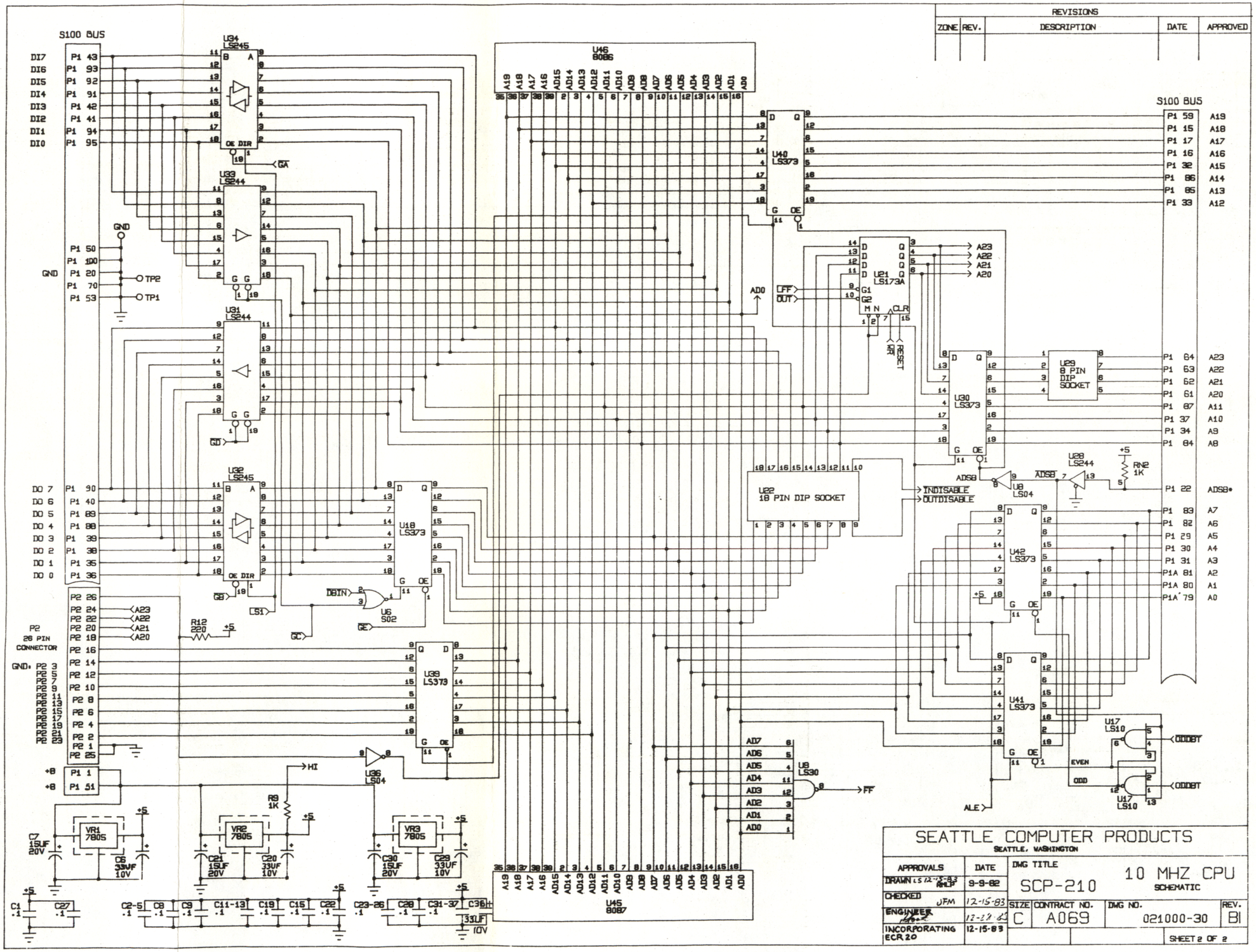
FRONT PANEL CONNECTOR

Socket U22 is provided for connection of an IMSAI type front panel to allow manual single step, etc. (must be properly software supported). This socket contains the signals INDISABLE* and OUTDISABLE* which disable the CPU regular bus controls to allow setting of starting addresses and data.

APPENDIX A. SCHEMATIC

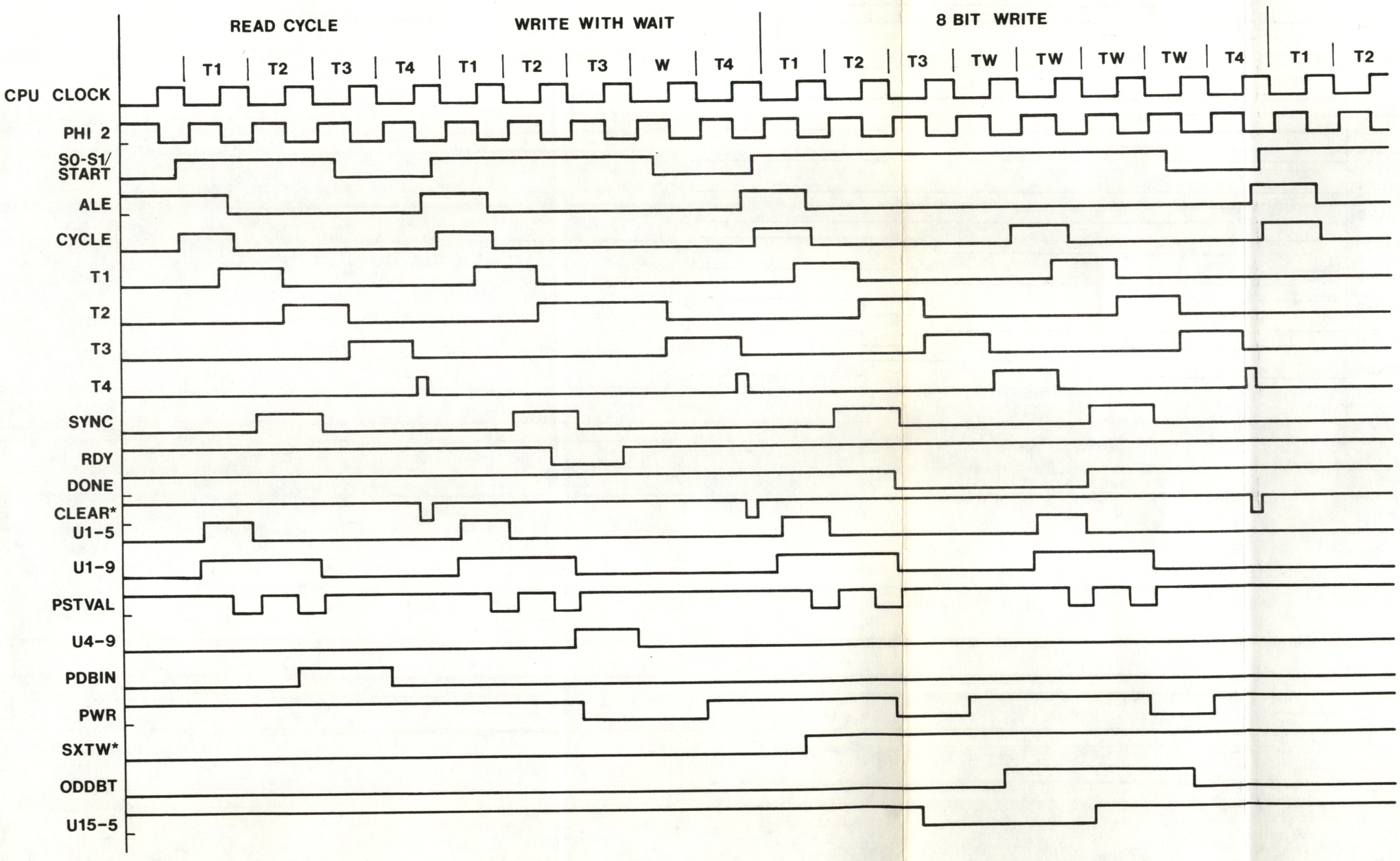


Schematic

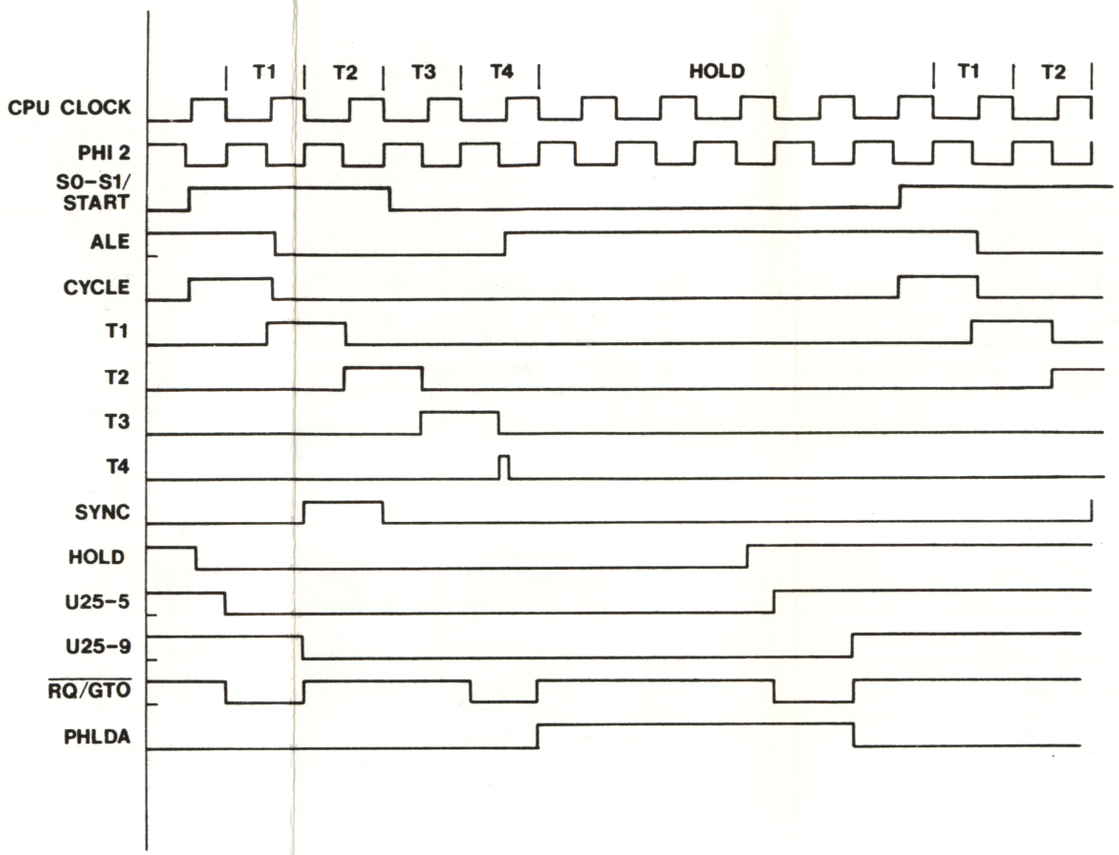

REVISIONS
ZONE | REV. | DESCRIPTION | DATE | APPROVED
S100 BUS
U46 8086
U34 LS245
U33 LS244
U31 LS244
U32 LS245
U40 LS373
U21 LS173A
U30 LS373
U29 8 PIN DIP SOCKET
U28 LS244
U22 18 PIN DIP SOCKET
U18 LS373
U42 LS373
U41 LS373
U39 LS373
U6 S02
U8 LS04
U8 LS30
U36 LS04
U17 LS10
U17 LS10
VR1 7805
VR2 7805
VR3 7805
U45 8087
P2 26 PIN CONNECTOR
RN2 1K
R12 220
R9 1K
SEATTLE COMPUTER PRODUCTS
SEATTLE, WASHINGTON
DWG TITLE
SCP-210
10 MHZ CPU
SCHEMATIC
APPROVALS
DRAWN
CHECKED
ENGINEER
INCORPORATING ECR 20
DATE
9-9-82
12-15-83
12-15-83
SIZE
C
CONTRACT NO.
A069
DWG NO.
021000-30
REV.
B1
SHEET 2 OF 2

APPENDIX B. TIMING DIAGRAMS

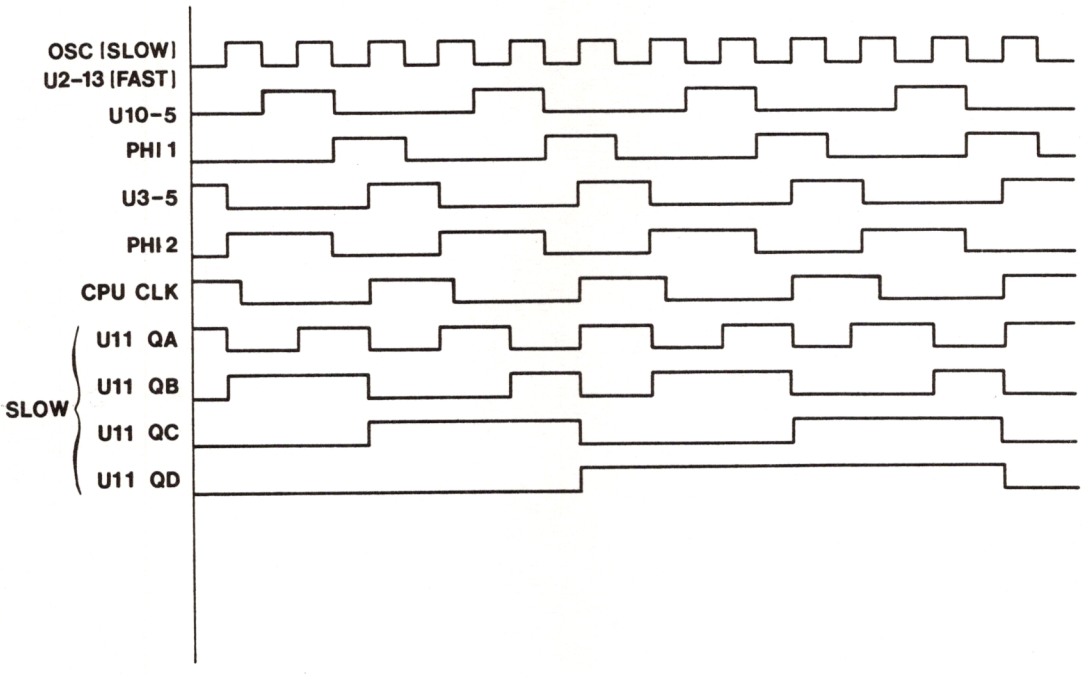
BASIC TIMING



HOLD TIMING


T1
T2
T3
T4
HOLD
T1
T2
CPU CLOCK
PHI 2
S0-S1/
START
ALE
CYCLE
T1
T2
T3
T4
SYNC
HOLD
U25-5
U25-9
RQ/GTO
PHLDA

SYSTEM CLOCK



APPENDIX C. 8087 OPTION

To install an 8087 chip on your CPU board, you may order Seattle Computer Products' 8087 package or buy an 8087 chip elsewhere.

The Seattle Computer Products' 8087 package includes a 5 MHz Intel 8087 Numeric Processor Chip along with this software:

- 8087 macros for the Microsoft Macro-86 assembler
- 8087 arithmetic routines for Microsoft or IBM BASIC compiler

This package may be ordered from Seattle Computer Products. The part numbers are:

Part Number	Size of Software Disk
0066001	8-inch disk
0066002	5-1/4-inch disk)

For additional information on the 8087 chip, see The 8086 Family User's Manual, Numerics Supplement from Intel.

APPENDIX D. SPECIFICATIONS

IEEE 696 Standard (S-100)	Fully compatible with the IEEE-696 specifications.
CPU Chip	8086-1 specified at 10 MHz. 8MHz version also available for use with 8 MHz 8087 numeric data processor.
Memory Capacity	Directly addresses 1 Megabyte (A0-A19). Address lines A20 through A23 are programmable to allow for 16 Mbyte addressability.
Memory Requirements	Static memory is recommended unless specifically designed for this CPU. Minimum memory access time for 10 MHz operation without wait states is 210 ns bus to bus.
Switchable Options	
Clock Speed	For the factory-provided 10 or 8 MHz CPUs, jumper selections provide for alternate half-speed operation, 5 or 4 MHz respectively.
Wait States	Four conditions: 1. One wait on all cycles; 2. One wait on memory cycles; 3. One wait on I/O cycles; 4. No waits.
8087 Interrupt	None, VI0-VI7, or NMI.
MWRITE	ON or OFF
SXTRQ	ON or OFF
High Address Lines	Address lines A20-A23 may be disconnected from the bus.

Specifications

Noise Margins	All signal inputs to the board have a minimum of 0.4V hysteresis at 25°C.
Power Requirements	8V, 1.2A nominal at 25°C.
Operating Environment	0°C to 70°C.
Reliability	Previous versions of this product have been in production and use for over three years, and have demonstrated typical reliability in excess of 98% per year.

Cut along line

Comment Form

Use this form to comment on this product and to report errors in the manual.

System Description:

CPU: Manufacturer _____ Model No. _____

Memory: Manufacturer _____ Model No. _____

Memory Size _____

Disk Controller: Manufacturer _____ Model No. _____

I/O Interfaces: Manufacturer _____ Model No. _____

Other _____

_____

_____

Comments:

Name _____ Company _____

Street _____

City _____ State _____ Zip _____

Phone _____ Date _____

Cut along line

Fold and tape

Place stamp here

Seattle Computer Products
1114 Industry Drive
Seattle, WA 98188

Attention: Hardware Support

Fold and tape

90-DAY LIMITED WARRANTY

WARRANTY AND WARRANTY PERIOD

When sold by Seattle Computer Products (hereinafter referred to as SCP) or through an authorized SCP dealer, this product is warranted to the original purchaser and all subsequent owners of the product for a period of 90 days from the time the product is first sold at retail and for such additional time as the product may be out of the owner's possession for the purpose of receiving warranty service at the factory. When sold to the end-user by an OEM, the warranty terms vary. Consult your OEM for specific warranty coverage.

WARRANTY COVERAGE

This product is warranted to be free from defects of material and workmanship and to perform within its specifications as detailed in the instruction or operating manual during the period of the warranty. This warranty does not cover damage and is void if the product has been damaged by neglect, accident, unreasonable use, improper repair, or other causes not arising out of defects in material or workmanship.

WARRANTY PERFORMANCE

During the warranty period, SCP will repair or replace defective boards or products or components of boards or products upon written notice that a defect exists. Certain high value parts may have to be returned to SCP prior to replacement. Other components will be replaced without the part having to be returned to the factory with the exception that SCP retains the right in all cases to examine the defective board or other products prior to the item's replacement under the warranty. In the event the return of the board, product, or component is requested by SCP under this warranty, the owner shall ship the item prepaid to the SCP factory. SCP will pay for shipment of replacement items back to the owner. All repairs or replacements under this warranty will be performed by SCP within five working days of receipt of notice of defect or return of components as called for under this warranty.

WARRANTY DISCLAIMERS

While high reliability was a major design factor for this product and care was used in its manufacture, no certainty can be achieved that any particular product will operate correctly for any specific time. No representation is made by SCP that this product will not fail in normal use. Because of the inability to guarantee 100% reliability, SCP shall not be liable for any consequential damage the user may suffer because the product fails to function reliably 100% of the time. Any implied warranties arising from the sale of this product are limited in duration to the warranty period defined above.

LEGAL REMEDIES

This warranty gives the purchaser specific legal rights. He may have additional rights which vary from state to state.

SHIPPING INSTRUCTIONS

In the event it becomes necessary to return the product or component to SCP:

1. Telephone (206) 575-1830 to obtain an RMA number. No products will accepted by SCP without an RMA number.

2. Package the product in a crushproof container with adequate packing material to prevent damage.

3. Return the product along with proof of purchase and a written explanation of the difficulty encountered along with your name, address, and phone number. Send the product to Seattle Computer Products, 1114 Industry Drive, Seattle WA 98188.